



Combined Cycle Engine Large-Scale Inlet for Mode Transition Experiments: System Identification Rack Hardware Design

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Acknowledgments

The work presented in this paper was funded by the NASA Fundamental Aeronautics Program Hypersonic Project. The authors sincerely appreciate the support and leadership of Dr. James L. Pittman, Langley, Hypersonic project principal investigator; Mr. Donald I. Soloway, Ames, Hypersonic project associate principle investigator for controls; Mr. Scott R. Thomas, Glenn, and Mr. Kenneth L. Suder, Glenn, CCE–LIMX project leads; Mr. John D. Saunders, Glenn, CCE–LIMX research lead; and Mr. John M. Koudelka, Glenn, hypersonic project manager. We also thank Bobby Sanders, TechLand, Lois Weir, TechLand, and the Glenn Facilities Division for tirelessly supporting this work. Furthermore, the authors wish to acknowledge the contributions made by Paul Raitano, Glenn, support engineer, in laying the groundwork for the buildup of the SysID Rack.

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This work was sponsored by the Fundamental Aeronautics Program at the NASA Glenn Research Center.

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Abstract

The System Identification (SysID) Rack is a real-time hardware-in-the-loop data acquisition (DAQ) and control instrument rack that was designed and built to support inlet testing in the NASA Glenn Research Center 10- by 10-Foot Supersonic Wind Tunnel. This instrument rack is used to support experiments on the Combined-Cycle Engine Large-Scale Inlet for Mode Transition Experiment (CCE-LIMX). The CCE-LIMX is a testbed for an integrated dual flow-path inlet configuration with the two flow paths in an over-and-under arrangement such that the high-speed flow path is located below the low-speed flow path. The CCE-LIMX includes multiple actuators that are designed to redirect airflow from one flow path to the other; this action is referred to as “inlet mode transition.” Multiple phases of experiments have been planned to support research that investigates inlet mode transition: inlet characterization (Phase-1) and system identification (Phase-2). The SysID Rack hardware design met the following requirements to support Phase-1 and Phase-2 experiments: safely and effectively move multiple actuators individually or synchronously; sample and save effector control and position sensor feedback signals; automate control of actuator positioning based on a mode transition schedule; sample and save pressure sensor signals; and perform DAQ and control processes operating at 2.5 KHz. This document describes the hardware components used to build the SysID Rack including their function, specifications, and system interface. Furthermore, provided in this document are a SysID Rack effectors signal list (signal flow); system identification experiment setup; illustrations indicating a typical SysID Rack experiment; and a SysID Rack performance overview for Phase-1 and Phase-2 experiments. The SysID Rack described in this document was a useful tool to meet the project objectives.

Nomenclature

AC	alternating current
A/D	analog to digital
BNC	Bayonet Neill-Concelman
CAD	computer-aided design
CAT 5e	category 5 enhanced cable
CCE-LIMX	Combined-Cycle Engine Large-Scale Inlet for Mode Transition Experiment
CDM	control design model
CPU	central processing unit
D/A	digital to analog
DAQ	data acquisition
DMSJ	dual-mode scramjet
DTL	development tools laptop
FAP	Fundamental Aeronautics Program
GB	gigabyte
FIFO	first-in-first-out

GNC	Guidance Navigation and Control
GUI	graphical user interface
HIL	hardware-in-the-loop
HMC	hydraulic machine controller
host	host laptop personal computer
HSFP	high-speed flow path
IBM	International Business Machines
IC	inlet characterization
I/O	input and output
ISA	industry standard architecture
LCD	liquid crystal display
LSFP	low-speed flow path
MFP	mass flow plug
NI	National Instrument
PCI	peripheral component interface
PFI	Precision Filters, Inc.
PHS	peripheral high speed
PID	proportional, integral, and derivative
PPC	Power PC
RALV	reuseable airbreathing launch vehicle
RTI	Real-Time Interface
SDRAM	synchronous dynamic random access memory
SPDT	single-pole, double-throw
SRPR	SysID Rack permissive relay
S/s	samples per second
S_{ti}	stability transient index
SysID	System Identification (Rack)
target	target rack-mount computer
TBCC	turbine-based combined-cycle
UEI	United Electronic Industries
USB	universal serial bus
VGA	video graphics array
10×10 SWT	10- by 10-Foot Supersonic Wind Tunnel

Introduction

NASA has invested in the research and development of safe, reliable, and controlled hypersonic flight (Ref. 1) for access to space. To this end, NASA has an interest in a two-stage-to-orbit vehicle concept. The propulsion system for the first stage will accelerate the vehicle from horizontal takeoff to a staging point at hypersonic speed. At the staging point, the two stages will separate and autonomously proceed to complete their missions. The NASA Fundamental Aeronautics Program (FAP) Hypersonics Project is concentrating on reusable airbreathing launch vehicle (RALV) missions (Ref. 1). The RALV missions warrant fundamental research of turbine-based combined-cycle (TBCC) (Ref. 1) propulsion systems that employ an integrated dual flow-path inlet with variable geometry to regulate airflow to a turbine engine and a dual-mode scramjet (DMSJ) (Ref. 2) combustor. Figure 1 illustrates a concept TBCC propulsion

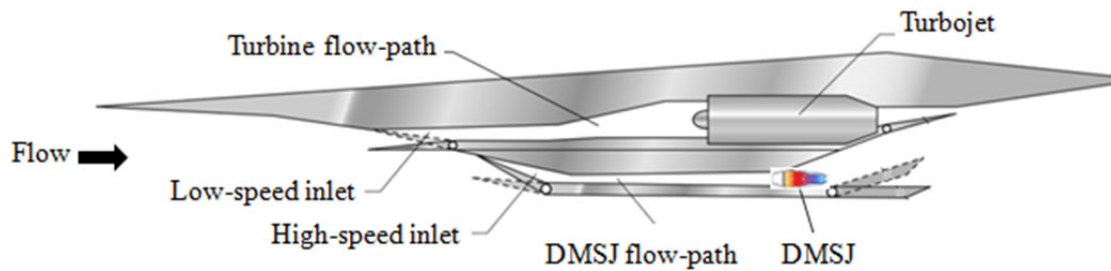


Figure 1.—TBCC propulsion system with a dual flow-path inlet in over-under arrangement.

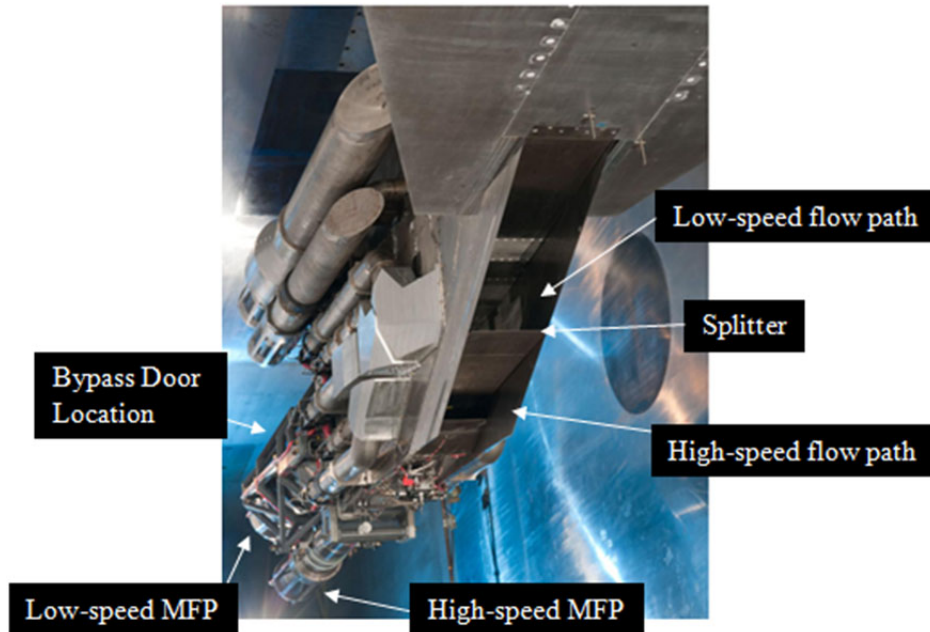


Figure 2.—CCE-LIMX testbed mounted in Glenn 10×10 SWT test section with key design features identified with labels.

system with a dual flow-path inlet configured in an over-under arrangement. For accelerating this vehicle from takeoff to supersonic flight, the low-speed inlet will be open to direct airflow to a turbojet. For further acceleration to hypersonic speed, the airflow will be directed to the DMSJ. The act of redirecting airflow from one engine to another is termed “inlet mode transition.”

Inlet mode transition is identified as one of the most critical TBCC-enabling technologies in the National Institute of Aerospace study (Ref. 3). To meet this challenge, NASA designed and built a Combined-Cycle Engine Large-Scale Inlet for Mode Transition Experiment (CCE-LIMX) testbed for ground testing in the NASA Glenn Research Center 10- by 10-Foot Supersonic Wind Tunnel (10×10 SWT) (Ref. 2). The CCE-LIMX testbed is an integrated dual flow path in an over-under configuration with the low-speed flow path (LSFP) and turbine located above the high-speed flow path (HSFP) and DMSJ. For Phase-1 and Phase-2 experiments, a mass flow plug (MFP) and cold-pipe assembly is used in place of a turbine engine while another MFP and cold-pipe assembly replaces the DMSJ. For these tests, cold pipes and MFPs are used to simulate the impact of a turbine and DMSJ on the inlet flow paths (Refs. 4 to 5). Figure 2 shows the CCE-LIMX testbed mounted in the test section of the 10×10 SWT.

Figure 3 is a computer-aided design (CAD) drawing that illustrates the CCE-LIMX mounted in the 10×10 SWT test section. As illustrated in Figure 3, the CCE-LIMX inlet system includes the following nine actuators: variable ramp; rotatable splitter; rotatable high-speed cowl; linear transitioning low-speed MFP; linear transitioning high-speed MFP; and four LSFP overboard bypass doors that are spaced 90°

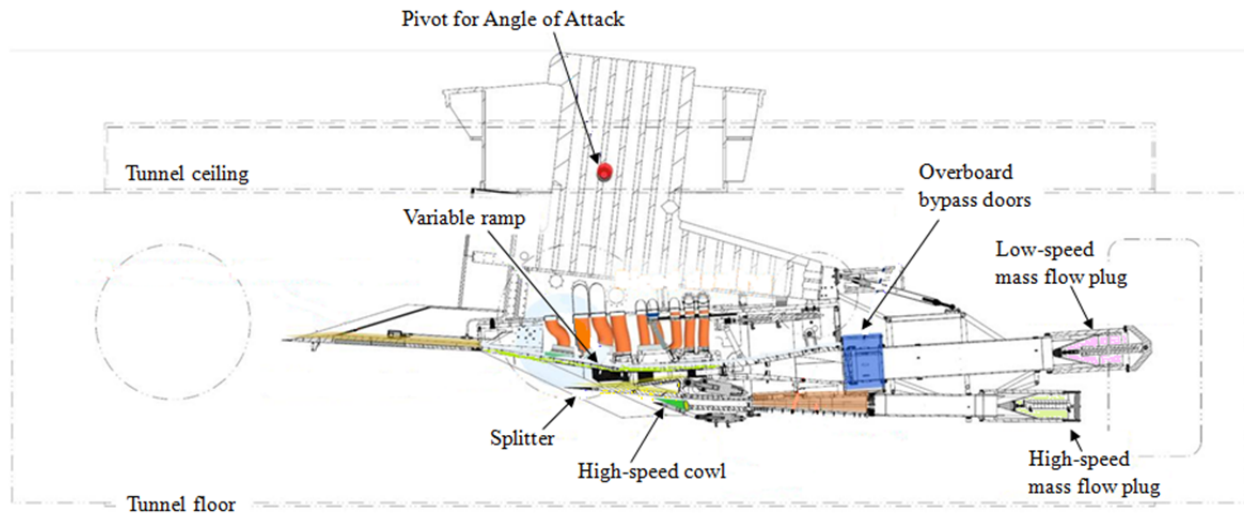


Figure 3.—CCE-LIMX testbed as mounted in the 10×10 SWT test section. Wind tunnel features are illustrated with dashed lines, CCE-LIMX significant design features and effectors are highlighted and labeled, and the wind tunnel airflow is from left to right.

apart at the aft end of the LSFP diffuser (Refs. 2 and 3). The ramp surface can be raised or lowered to increase or decrease the throat area. The splitter serves both flow paths. The upper surface of the splitter serves as a low-speed cowl surface and the lower surface of the splitter serves as part of the high-speed ramp surface. The high-speed cowl can be rotated to change the air capture area for the HSFP. The MFPs are mechanisms to pressurize the inlet. The overboard bypass doors are used to vent air from the LSFP, upstream of the cold pipe, to simulate dynamic disturbances originating from the turbine. The ramp, upper surface of the splitter, four bypass doors, and the low-speed MFP are effectors for the LSFP. The HSFP effectors are the high-speed cowl, high-speed MFP, bottom surface of the splitter, and to a lesser degree the ramp. The inlet system geometry is defined by the positions of these actuators. The CCE-LIMX is mounted on a strut that can be rotated about a pin to change the angle of attack.

The progressive course for testing the CCE-LIMX in the 10×10 SWT is segmented into multiple test phases (Refs. 2 and 8) starting with steady-state inlet performance assessments and moving forward to tests that include a turbine engine at the aft end of the LSFP. For the first phase of testing, Phase-1, efforts focused on aerodynamic inlet characterization (IC) experiments. Information gathered from Phase-1 testing will be used in the process for shaping mode transition schedules. The mode transition schedules yield a course of inlet system geometries, at each incremental step, as the inlet reconfigures while performing mode transition. Each incremental step on the inlet mode transition schedule is a mode transition operation point. IC involves studying the many pressure sensors, static and high-speed, located within the CCE-LIMX flow paths at various operating points. Phase-2 system identification experiments are prerequisite for development of closed-loop controllers that consider system dynamics and potential disturbances as the inlet transitions to and functions at and about the mode transition operating points identified from Phase-1 experiments. Specifically, Phase-2- type research determines the dynamic response of the airflow through the inlet due to changes in actuator positions. Phase-3 is a controls experiment to demonstrate closed-loop control while performing mode transition.

To support data acquisition (DAQ) and control of the CCE-LIMX throughout all experiment phases, the FAP Hypersonic project Guidance Navigation and Control (GNC) team designed and developed a real-time DAQ and control instrument rack. Initially, the primary purpose of this instrument rack was to support Phase-2 system identification testing; therefore, this instrument rack is called the System Identification (SysID) Rack (Ref. 8). The control flexibility inherently designed into the SysID Rack made it useful to also support Phase-1 testing and will make the SysID Rack useful for Phase-3 testing and beyond.

The SysID Rack design enables the following capabilities: safely and effectively move multiple actuators individually or synchronously; sample and save effector set-point signals, effector feedback signals, and CCE–LIMX pressure sensor signals; automate control of actuator positioning based on a mode transition schedule; and perform the DAQ and control processes at 2.5 KHz.

The remaining sections of this document focus on the SysID Rack hardware and peripheral components assembled to meet CCE–LIMX testing requirements. The next few sections include how CCE–LIMX actuators are controlled, a physical description of the SysID Rack, SysID Rack hardware components and external peripheral components including their purpose and specifications, SysID Rack CCE–LIMX effector signal flow listing, and a SysID Rack experiment setup. Then, dynamic plots indicative of an experiment are presented in the SysID Rack experiment section. A SysID Rack performance section highlights how the SysID Rack performed during dynamic CCE–LIMX experiment testing. Finally, a summary of this work is provided.

CCE–LIMX Testbed Actuator Controls

In the 10×10 SWT test facility, the movement and positioning of all nine CCE–LIMX variable actuators are controlled with hydraulic machines. These machines include cylinders, piston heads, and piston rods. Hydraulic fluid flows into and out of the cylinder to vary the force applied to the cylinder piston, which in turn will either linearly increase or decrease the extension of the piston rod out of the cylinder. Servovalves used to control fluid flow into and out of the cylinders are regulated with proportional, integral, and derivative (PID) hydraulic machine controllers (HMCs). For Phase-1 and Phase-2 tests, the integral and derivative gains of the HMCs were zero. The HMC determines control signals for the servovalves based on a weighted difference between a set-point signal and a feedback signal indicative of the length of the hydraulic piston rod extension. The set-point and feedback values are from external sources, ranging from 0.0 to +5.0 V, and they are applied to a set-point port and a feedback port on the HMC. Signals applied to the HMC set-point ports are controlled from within the 10×10 SWT control room (Ref. 6). The control room employs a digital system with a graphical user interface (GUI) to adjust the voltage values applied to the HMC set-point ports. The feedback signal is from the wiper of a potentiometer configured as a variable voltage divider. One end of the potentiometer resistive element is at 0.0 V, the other is at +5.0 V, and the wiper was physically fastened to the piston rod. For these tests, the potentiometers had two resistive elements. One resistive element was dedicated to applying feedback signals for the HMC and the other was available for research.

All SysID Rack data acquired is saved at a rate of 2.5 KHz. The 2.5 KHz rate was determined to enable capturing and responding to disturbances created by the fastest moving mechanical actuator on the CCE–LIMX testbed, the bypass doors (Ref. 8). These doors were designed to introduce disturbances in the LSFP within the 0 to 100 Hz frequency range. Precision Filters, Inc. (PFI), instruments, programmed as low-pass filters, signal condition all analog feedback signals available to the SysID Rack. The filtered signals are the products of an 8th order Bessel transfer function designed to have a 200-Hz cutoff frequency. These signal conditioners served as anti-aliasing filters to reduce foldover frequencies that may corrupt the digitized data. The product of signals applied to the Bessel function filters are recorded with the SysID Rack. The anti-aliasing filter design can be found in the appendix of Reference 8.

SysID Rack Overview

The SysID Rack, as illustrated in Figure 4, is a collection of hardware components assembled in an instrument rack to support all phases of the CCE–LIMX mode transition experiments. To meet the project needs, the SysID Rack was designed and developed with multiple computational components to perform tasks beyond the capabilities of the system employed in the 10×10 SWT facility control room. Essentially, all CCE–LIMX actuators have the following two sources for the HMC set-point ports: the SysID Rack and the facility controller. A facility controller and SysID Rack permissive relay (SRPR)

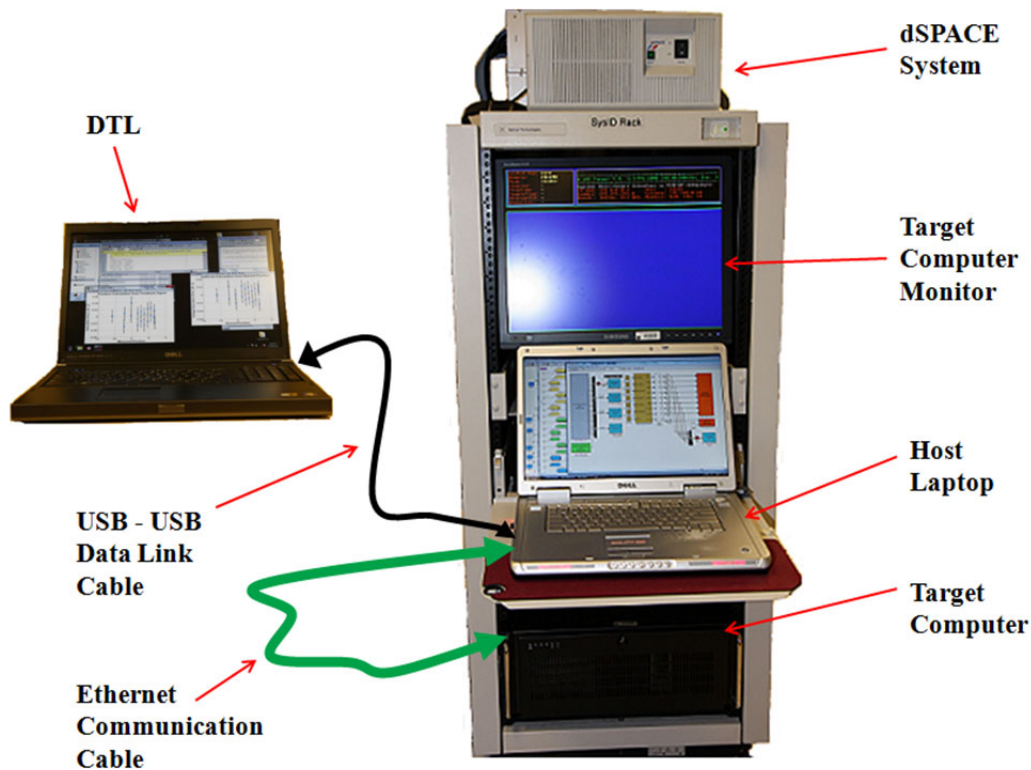


Figure 4.—SysID Rack is a system that includes the following four interconnected computational components: dSPACE system, target, host, and development tools laptop.

switching network panel is used to select which signal is applied to the HMC set-point ports. The SRPR panel is a bank of single-pole, double-throw (SPDT) relay switches located in a facility wiring cabinet. Nine control signals from the control room and nine control signals from the SysID Rack are applied to the SRPR source gates. The nine SRPR load gates are hardwired to the HMC set-point ports for each of the CCE–LIMX effectors. Experiment control is transferred by way of an operator controlling the states of the SRPR panel contacts, individually or simultaneously.

The following are the three primary computational components employed in the SysID Rack: host laptop computer with a convenient docking station or port replicator, real-time target computer (i.e., rack-mount computer or target) that includes DAQ boards mounted on the motherboard inside the target box, and a real-time dSPACE (dSPACE GmbH) system that also includes DAQ boards. The host is the programming platform for developing all code that defines the target and dSPACE processes. Also, the host is a user gateway for controlling the SysID Rack. The target process, designed to continuously run, receives experiment instructions from the host, calculates HMC set-point values for all CCE–LIMX effectors, records all actuator control and feedback signals, records all pressure sensor signals, and can transmit real-time information back to the host. All recorded signals are saved in a target file that is available to be downloaded to the host. The dSPACE process, which serves as a redundant throughput device for risk reduction purposes, relays the target signals to the HMCs. Custom code has been written to define the processes of the host, target, and dSPACE system.

The hardware components include the host, target, dSPACE, component interface wiring, a development tools laptop (DTL), and a monitor for the target. The instrument rack is a mobile “half height” (5-ft-tall) cabinet equipped with the following features and accessories:

- Vented side and top panels
- One rear-locking vented door
- Three 2-in.-diameter cable feedthrough holes

- Four 3-in.-diameter heavy-duty casters
- Four leveling screws
- One retractable keyboard shelf
- Three support shelves
- One master power rocker switch with light-emitting diode power on indicator
- One 110-V alternating current (AC) power distribution unit

The target monitor, used to display real-time status of the target executable as well as the real-time operating system status, is directly connected to the video graphics array (VGA) 15-pin D-subminiature connector on the target. Two panels mounted inside the cabinet behind the back door are not illustrated in Figure 4. The first panel is a target DAQ interface panel that includes multiple breakout screw terminal junction boards. These boards are connected, by way of commercial off-the-shelf cables, to the target DAQ boards. The second panel is a dSPACE reset panel that includes a momentary push button, +5.0-V power supply, and a power-on contact switch.

For this assembly of components to be functional as an experimenting resource, communication between components is essential. Figure 5 is a signal flow illustration to show how hardware components are interfaced. Host-target cross communication employs an Ethernet connection. Communication between the target and dSPACE system is via DAQ boards. The screw terminal boards provide a convenient way for the target to interface with the dSPACE DAQ boards and the PFI signal conditioners. A fourth computational component associated with the SysID Rack is the DTL. A GO! Suite (Ours Technology, Inc.) universal serial bus (USB)–USB data link is used to facilitate communication between the host and the DTL. Code developed on the host defining the dSPACE system process is downloaded to the dSPACE computer via fiber-optic cable; because this code is downloaded once and the fiber-optic cable then removed, this cable is not represented in Figure 5.

The next several subsections describe the computational devices associated with the SysID Rack. These sections will provide overview information describing each of the SysID Rack computational components along with their functions, specifications, and system interfaces.

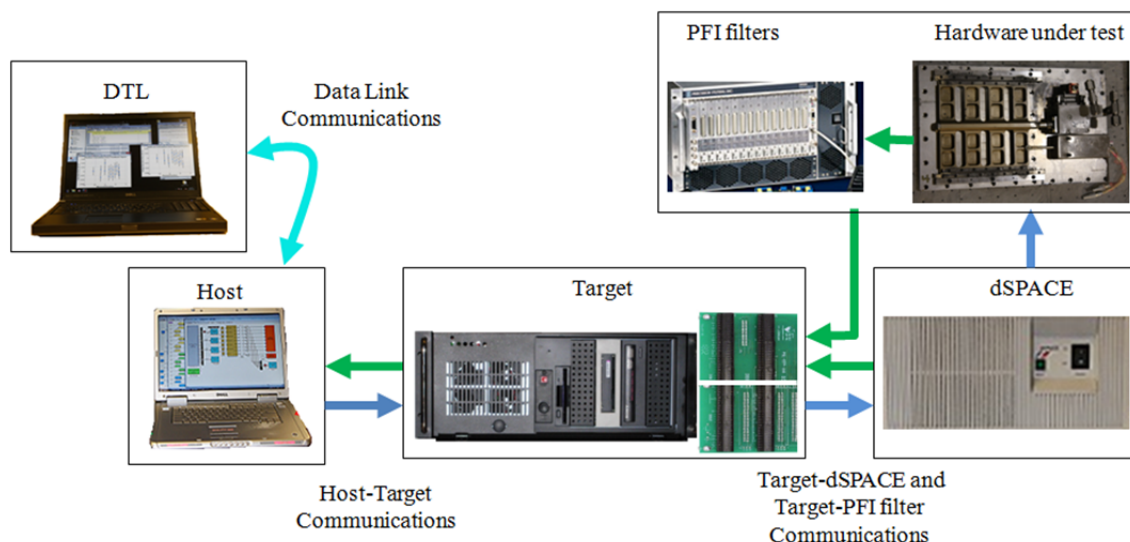


Figure 5.—SysID Rack hardware component and signal flow illustration. CCE–LIMX actuator control signals generated from the host are represented by the blue arrow while feedback signals are identified by the green arrow. The cyan arrow identifies the host and DTL communication interface for file exchange.

Target Overview

The target process is designed to run continuously and perform the following tasks within each time step: determine HMC set-point signals based on host instructions, apply signals to digital-to-analog (D/A) ports, record all signals applied to the target analog-to-digital (A/D) ports to memory, and send signals pertaining to the signals from the actuator position feedback sensors to the host for display. Signals applied to the D/A ports pertain to the desired signal to be applied to the HMC set-point ports and a +5.0-V signal on a sense line. A signal on the sense line less than +5.0 V will indicate a failed target; such an event will most likely require rebooting the target. The target A/D ports sense the signals processed by the PFI signal conditioners and the nine control signals from the SysID Rack that are applied to the SRPR source gates.

The target (Ref. 8) is an industrial rack-mounted computer configured with the MATLAB real-time xPC Target (The MathWorks, Inc.) operating system (version 3.4) to enable running real-time hardware-in-the-loop (HIL) applications. The target comprises the following components:

- 2.0-GHz Intel Pentium (Intel Corporation) dual-core processor
- 4.0-gigabyte (GB) RAM
- Standard 3.5-in. floppy disk drive
- The following xPC Target compatible DAQ A/D and D/A boards:
 - United Electronic Industries (UEI) high-performance high-speed DAQ A/D peripheral component interface (PCI) board (PD2–MF–64–500/16H)
 - PD–CBL–96 transmission cable
 - PD–STP–96 screw terminal board
 - Two National Instruments Corporation (NI) high-performance high-speed DAQ D/A PCI boards (PCI–6733)
 - SH68–68–EMP transmission cables for each
 - SCB–68 screw terminal boards for each
- I8254X Ethernet controller board
- External liquid crystal display (LCD) monitor

Table 1 lists the target computer hardware component specifications that meet the SysID Rack design requirement. A 2.0-GHz processor was selected to ensure that custom application code can be processed without causing a central processing unit (CPU) overload condition, also known as a target failure. The size of the RAM memory is suitable for running the target process and storing all recorded data in real time. The xPC Target operating system resides on a 1.44-MB, 3.5-in. floppy disk, which is needed to read the 1.44-MB, 3.5-in. floppy target boot diskette. All target DAQ boards were selected to meet or exceed xPC Target minimum requirements as specified by The MathWorks, Inc. The Ethernet card is used to enable communication between the target and host. Finally, the target 20-in. flat-panel monitor is used to display select information pertaining to the target process. Table 2 is a list of monitor specifications. Figure 6 illustrates the target hardware signal wiring connections.

The target process code development used Real-Time Interface (RTI) library xPC input and output (I/O) blocks with ports that are linkable to other blocks available with the MATLAB Simulink (The Mathworks, Inc.) software. The target code is compiled and downloaded from the host over the Ethernet using Real-Time Workshop software.

In Table 1 the target hardware component specifications meet or exceed requirements to run the target's real-time HIL processes. The target's bus architecture supports the PD2–MF–64–500/16H and PCI–6733 PCI adapter boards and the I8254X Ethernet controller card. The 3.5-in. floppy disk drive enables loading and running the target operating system from a boot floppy disk.

TABLE 1.—TARGET HARDWARE COMPONENT SPECIFICATIONS

Target	Specifications
CPU	Dual core 2.0 GHz
RAM	4.0 GB
Drive	Hard drive: 150.0 GB
Drive	3.5-in. floppy disk
Drive	CD–RW/DVD ROM
PCI adapter	One PD2–MF–64–500/16H United Electronics International (UEI) data acquisition (DAQ) adapter
PCI adapter	Two PCI–6733 NI DAQ adapters
PCI Ethernet card	I8254X with fast gigabit Ethernet controller

TABLE 2.—TARGET MONITOR SPECIFICATIONS

Target monitor	Specifications
Monitor type	LCD monitor
Screen size	20.1 in.
Resolution	1600.0 by 1200.0 pixels
Product dimensions (height by width by depth)	17.6 by 15.4 by 8.7 in.
Product weight	16.8 lb
Connector	VGA
Horizontal viewing angle	178.0°
Vertical viewing angle	178.0°

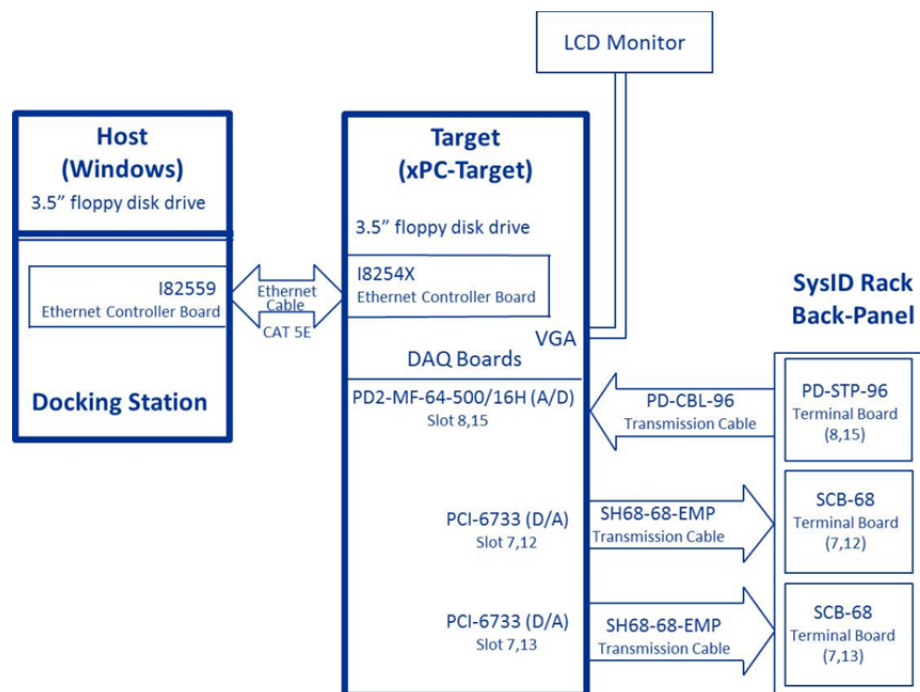


Figure 6.—Target hardware signal interface schematic. Target I8254X and host I82559 Ethernet controller boards enable bidirectional communications/data flow via an Ethernet cable. An LCD monitor provides a means to view the status of a target real-time application process. The PD2–MF–500/15H A/D board is linked to a PD–STP–96 screw terminal board by way of a PD–CBL–96 transmission cable. Ultimately, this transmission cable is used to transmit feedback signals to the target. PCI–6733 D/A boards are used as the medium that transmits control signals to SCB–68 screw terminal boards via SH68–68–EMP transmission cables.

In Table 2 the target monitor's specifications, monitor type, screen size, resolution, viewing angle, and featured accessories more than meet the requirement for viewing and monitoring the target real-time operational status.

Booting the target with the 3.5-in. floppy diskette inserted in the disk drive will load and start the xPC Target 3.4 real-time kernel and enables an application loader. The real-time kernel provides a means to dedicate all target resources to the HIL application while reducing the CPU usage of nonessential target functions (power saving features, keyboard, mouse maintenance, etc.). I/O hardware is linked to the real-time kernel by means of kernel built I/O addresses. The I/O addresses are used by software drivers supported by xPC Target block library driver sets to interact with target D/A and A/D boards.

Target Hardware and Peripherals

The specifications for the target I/O boards are listed in Table 3. The PD2–MF–64–500/16H A/D I/O board provides 16-bit resolution; 500 K samples per second (S/s) sampling rate; programmable gains of 1, 2, 4, or 8; and 64 single-ended channels. The A/D board ports are configured with a voltage range of 0.0 to +5.0 V. The board is interfaced with a PD–STP–96, a 64 connection I/O screw terminal board via PD–CBL–96 high-speed analog data transmission cable. All analog, feedback, and signals to be recorded by the SysID Rack are hardwire connected to the PD–STP–96 screw terminal board.

Each of the PCI–6733 D/A boards provides 16-bit resolution, 1-M S/s update rate, ± 10.0 -V output range, and eight analog single-ended channels. These boards simultaneously provide signals pertaining to the desired positions of the nine CCE–LIMX actuators, along with a target failure signal, that are sensed by the dSPACE system. The target failure signal is also sensed by a 10 $\times$ 10 SWT facility annunciator alarm panel. The SH68–68–EMP shielded 68 pin cables with individually wrapped twisted pair conductors to reduce crosstalk on high-speed data transmission lines that are used to connect the PCI–6733 boards to NI SCB–68 I/O screw terminal boards. NI SCB–68 I/O screw terminal boards are shielded by 68 pin low-noise signal I/O devices. SCB–68 contacts are hard wired to dSPACE A/D channels.

In Table 3 the PD2–MF–64–500/16H A/D board provided the necessary bit resolution, number of single-ended channels, gain capability, input voltage range (0.0 to +5.0 V), and sample rate capability for acquiring CCE–LIMX dynamic feedback data. Two PCI–6733 D/A boards are equipped with a ± 10.0 -V range, a sampling rate between 740 K and 1-M S/s, and eight single-ended channels per board (among other specifications). The PD2–MF–64–500/16H and PCI–6733 board features enable the SysID Rack to receive feedback signal as well as transfer output command signals.

TABLE 3.—UNITED ELECTRONICS INTERNATIONAL (UEI) A/D AND NATIONAL INSTRUMENT (NI) D/A PCI BOARD SPECIFICATIONS

Target peripheral	Specification
PD2–MF–64–500/16H	PCI bus
	64 single-end channels
	16-bit resolution
	1, 2, 4, and 8 gains selection
	Analog input range: 0 to 5, ± 5 , and ± 10 V
	16-bit A/D size
	Sampling rate 500-K S/s
	2-K byte A/D first-in–first-out (FIFO) size
	Transfer size normal modes: 1024-K byte
PCI–6733	PCI form factor
	Eight single-end channels
	16-bit resolution
	Analog input range: ± 10 V
	16-bit A/D size
	Sampling rate: 740-K to 1-M S/s
	A/D FIFO size: 16-K samples
	Update rate of local FIFO: 740-K S/s

The PCI Ethernet card identified in Table 1 is a high-data-throughput network communication board with a fast gigabit Ethernet controller installed. The Ethernet network includes a serial high-speed Ethernet network communication crossover cable, category 5 enhanced cable (CAT 5E). Ethernet technology allows bidirectional data exchange on its data bus at high data throughput rates (100 Mbits/sec or 1000 Mbits/sec).

dSPACE System Overview

The dSPACE process senses signals on the A/D ports from the target D/A boards and from the momentary push button on the dSPACE reset panel. The dSPACE process also applies signals on D/A ports that are hardwired to the SRPR source gates, which in turn are channeled to the HMC set-point ports. These signals are also available to the target A/D ports. Essentially, the dSPACE process is a transparent interface between the target and the HMCs. For normal operation, the dSPACE process reads the target signals (± 10.0 V), scales the signals to values within a 0.0- to +5.0-V range, and applies the scaled values as a signal set to dSPACE D/A ports. To reduce risk of sending errant signals to the HMC in the event of a target failure, the dSPACE system can reject subsequent signals from the target while maintaining a previous signal set on the D/A ports. The concern is that a target fault may result in signals that will lead to repositioning the CCE–LIMX actuators to nonscheduled and potentially unsafe positions. For example, if the target fails to maintain real-time processing of its code, it will experience a system crash that results in all target D/A ports changing to 0.0 V. This can result in a step change for one or more HMC set-point signals. A nonscheduled actuator step change is a dangerous scenario when the CCE–LIMX is immersed in supersonic airflow. Instead of one or more HMCs simultaneously receiving a set-point step change, a preferable course of action would have the signals maintained at their previous values until the error is resolved. Such a target failure will also change the sense-line signal to 0.0 V. If a sense-line step change is detected, previous signals on all dSPACE D/A output channels will be maintained indefinitely regardless of future target signals. The sense line is also wired directly to a set of facility annunciator relay contacts that will trigger an audio alarm and light an annunciator window. To resume normal operation after the error has been cleared, the dSPACE system is conveniently reset with a release signal from a momentary push button located on the dSPACE reset panel. Upon receipt of this step change signal, the dSPACE system process is programmed to unlatch and resume normal operation.

dSPACE System Hardware and Peripherals

The dSPACE system (Ref. 8) is a commercial-off-the-shelf computer with a real-time operating system and DAQ boards specifically designed for HIL applications. The following hardware components are included with the SysID Rack dSPACE system:

- PX10 rack mount expansion box or chassis
- DS1005 PowerPC (PPC) board provides computational capability for real-time applications and includes the following:
 - International Business Machines (IBM) PPC 750GX processor
 - industry standard architecture (ISA) bus
 - peripheral high-speed (PHS) bus for fast (16-Mbps transfer rate) communication with I/O boards that support PHS bus access
- DS814 personal computer to ISA bus interface board to interface with the host via fiber-optic cable—this communication path enables programs to be downloaded from the host
- DS2002 high-speed A/D converter board that receives signals from the following two sources:
 - Target D/A ports representing control signals for the actuator controllers
 - Momentary push button on the dSPACE reset panel

- DS2103 high-speed D/A converter board that applies dSPACE scaled control signals to the following:
 - SRPR panel source ports
 - Target A/D ports for recording the control signals

The dSPACE DAQ ports interface the dSPACE system with the target, dSPACE reset panel, and the SRPR panel. Ten D/A channels from the target, signals for the nine actuators, a sense line, and the signal from the dSPACE reset panel momentary push button are applied to a dSPACE DS2002 A/D by way of a Bayonet Neill-Concelman (BNC) connector panel designed to accommodate miniature quick connect and disconnect connectors for coaxial cable. The dSPACE A/D ports 1 to 9 are actuator control signals, port 10 is the sense line, and port 11 is the release signal. The dSPACE output ports on the DS2103 D/A board are connected to both the SRPR panel source ports by way of another BNC connector panel and to the SysID Rack target screw terminal boards.

Similar to the process used to develop code for the target, the dSPACE process control code is developed using The MathWorks, Inc., Simulink software. The dSPACE provides the RTI library that includes dSPACE A/D and D/A I/O blocks with ports that are linkable to other blocks available with the MATLAB Simulink software. The code is developed and compiled on the host and downloaded to the dSPACE processor using MathWorks Real-Time Workshop (The MathWorks, Inc.) software over a fiber-optic cable. Table 4 shows the hardware component specifications for the dSPACE PX10 system and Figure 7 illustrates the dSPACE hardware wiring schematic.

In Table 4 the dSPACE system is enclosed in a PX10 expansion box (chassis) equipped with a bus architecture that accommodates a DS1005 PPC board, DS2002 A/D board, DS2103 D/A board, and DS814 link board.

TABLE 4.—THE dSPACE SYSTEM HARDWARE COMPONENT SPECIFICATIONS

dSPACE system	Specification
dSPACE PX10 expansion box	10 full-size 16-bit ISA slots
	90 to 264 V auto ranging source alternating current (AC) power supply, 550 W
	Fan cooling
DS1005 Power PC (PPC) board	IBM PPC 750GX 1.0 GHz
	L1 data cache 32 KB
	L1 instruction cache 32 KB
	L2 cache 1 MB
	16-MB flash memory
	128 MB synchronous dynamic random access memory (SDRAM)
	ISA bus
	PHS and PHS++ I/O board bus
DS814 link board	Host to ISA bus interface
	Fiber optic 100 Mbits/s
DS2002 A/D board	32 channels
	16-bit (programmable for 4-, 8-, 12-, or 16-bit) resolution
	± 10 -V (programmable for ± 5 or ± 10) input volt range
	Two independent A/D converters
	Sampling time about 5.0 μ s per two channels; approximately 93.5 μ s for all 32 channels (16 bit)
	High-speed communication PHS bus
	ISA bus
DS2103 D/A board	32 parallel D/A channels
	14-bit resolution
	± 5 -V (programmable for ± 5 or ± 10) output volt range
	10.0 μ s sampling time
	High-speed communication PHS bus
	ISA bus

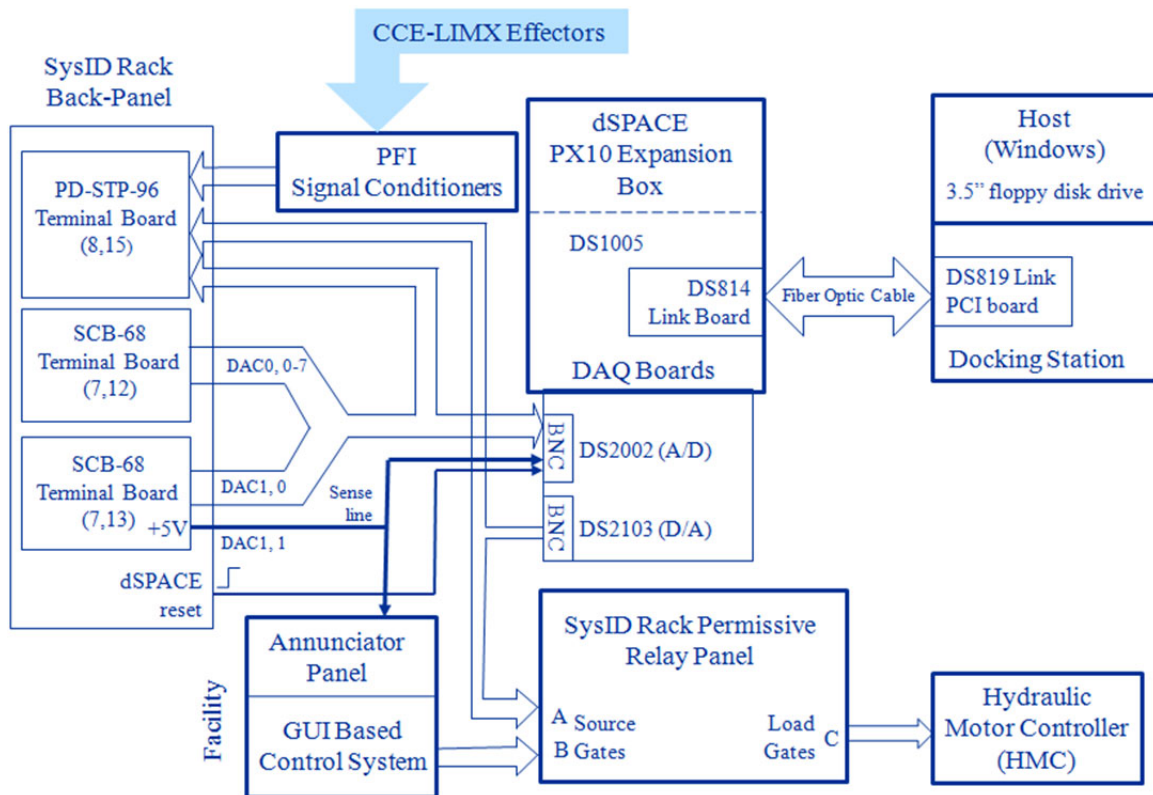


Figure 7.—The dSPACE system is interfaced with the host, SysID Rack, 10×10 facility annunciator (relay) panel, and a 10×10 facility SysID Rack permissive relay (SRPR) panel. The dSPACE and host communicate over a fiber-optic cable. The dSPACE DS2002 board senses signals from the SysID Rack, control signals originating from the target, and a reset signal. The dSPACE DS2103 D/A board is wired to both the SysID Rack PD-ST-96 terminal board and the 10×10 facility control room SRPR panel.

Host Overview

Custom software that defines the host process, which includes a GUI and a host model, is developed using The MathWorks MATLAB and Simulink software. For typical SysID Rack operation, custom software developed for running on the host process enables a user to start or stop the target process, send instructions to the target process, receive feedback signals from the target, display target signals on a monitor, and retrieve experiment data files from the target. An operator uses the host to set up the target process by sending instructions via the Ethernet to perform specific tasks, as required to satisfactorily and safely perform experiments on the CCE-LIMX. When receiving an experiment data file from the target, the host process will automatically determine a unique filename for the data set that is saved on the host hard disk. Data files on the host can be passed to the DTL using the GO! Suite USB-USB data link system.

The host is a laptop computer that employs the Windows Vista (Microsoft) graphic-based operating system with the following specifications: a 2.33-GHz dual core processor, 175.0-GB hard drive memory storage device, and 4.0-GB RAM. The host is also configured with an external 3.5-in. floppy disk drive, an I82559 Ethernet adapter card, an external docking station, and a GO! Suite USB-USB data link cable system. The floppy drive is used to create a target floppy boot diskette. The Ethernet card is used to link, through the docking station, the host to the target via the Ethernet cable. The host is mounted on an external laptop docking station with a convenient connection for the Ethernet cable.

Host is equipped with the following software products:

- MathWorks software includes the following products:
 - MATLAB
 - Simulink
 - MATLAB Real-Time Workshop
 - xPC Target 3.4
- Microsoft Office includes Word and Excel
- Visual Studio (Microsoft) 2005 C compiler

Host Hardware and Peripherals

Table 5 lists the hardware and peripheral specifications for the host.

The docking station is an AC-powered peripheral device used to convert the mobile host into a single location desktop computer. When the host is mounted in the docking station, the docking station isolates the host from “hard” or direct AC power surges that may occur during a host power startup. Table 6 shows the docking station hardware specifications.

This 5-ft-long data transfer cable, listed in Table 7, supports the USB 2.0 data protocol. The host and DTL run supported operating systems Vista and Windows XP, respectively. With the USB to USB cable, the host is connected to the DTL for bidirectional file exchange.

TABLE 5.—HOST HARDWARE SPECIFICATIONS

Host	Specifications
CPU	Dual core 2.33 GHz
RAM memory	4.0 GB
Hard drive	175.0 GB at 7200.0 rpm
Monitor	17.0 in.
Network adapter	I82559 with fast gigabit network controller

TABLE 6.—THE HOST DOCKING STATION OR PORT REPLICATOR IS AN ACCESSORY THAT THE HOST EASILY PLUGS INTO AND OUT OF. THIS DOCKING STATION PROVIDES PORTS FOR EXTERNAL HARDWARE CONNECTIONS SUCH AS A MONITOR, USB PERIPHERALS, AND NETWORK DEVICES

Host docking station	Specifications
Weight	6.6 lb
Dimensions (height by width by depth)	2.1 by 10.9 by 5.6 in.
USB I/O connector	Three standard USB powered and one USB
Video I/O connector	VGA
Network connector	10/100/1000 GB Ethernet
AC adapter power supply	110 VAC, 50 to 60 Hz, and 1.5A maximum
Controls	Power button (on/off)

TABLE 7.—GO! SUITE USB TO USB DATA TRANSFER CABLE SPECIFICATIONS

Data transfer cable	Specifications
Connector type(s)	Two USB A Male, 4 pin
Data transfer rate	USB 2.0, 480 Mbps
OS support	Windows 2000/XP/Vista/7, 32 and 64 bit
Cable length	5 ft (1.52 m)

Development Tools Laptop

The following are the two main functions of the DTL: first, is to reduce, analyze, and store experiment data. Through a USB port the DTL can transfer files via the USB-to-USB data transfer cable between the DTL and the host. Second, DTL software tools were developed to support the SysID Rack calibration process.

The DTL is a personal computer compatible laptop with standard hardware and a graphics-based operating system (Ref. 8). The DTL employs a 2.0-GHz quad core processor, 175.0-GB hard drive, 8.0-GB RAM, and an open USB port. See Table 8 for the DTL hardware specifications. Loaded software includes The MathWorks MATLAB and Simulink software and Microsoft Office software.

TABLE 8.—DEVELOPMENT TOOLS LAPTOP SPECIFICATIONS.
THIS LAPTOP COMPRISES A STANDARD CPU,
RAM, HARD DRIVE, AND USB PORT

DTL	Specifications
CPU	Intel Core i7-920 Quad Core at 2.0 GHz
RAM	8.0 GB at 1600.0 MHz
Hard drive	175.0 (GB) at 7200.0 rpm
Port	USB

SysID Rack Signal Flow

The SysID Rack is interfaced to 29 CCE–LIMX testbed effectors, 9 actuators, and 20 pressure signals. Signal flow tables were established to identify which D/A port channels connect to each effector, in what order data is saved in the data files, and to define the signals applied to each target A/D ports.

The signal flow tables and their naming nomenclature is discussed and identified in the appendix section of this document.

SysID Experiment Setup

Prior to running experiments with the SysID Rack, the target signals need to be calibrated with respect to manually measured CCE–LIMX actuator positions. The calibration step is necessary to translate signals in units of voltage to values in engineering units. The calibration process, considering one actuator at a time, involves applying a voltage signal to the HMC set-point port, manually measuring and taking note of the resultant actuator position, and using the target to record the actuator feedback signals. This data set is then reduced to calibration curves for each actuator and incorporated into the target process.

After all software is developed to run on the host, target, and dSPACE, all hardware connections are established, as illustrated in Figures 6 and 7, and the SysID Rack has been calibrated, the preparation process for readying the SysID Rack to perform system experiments on the CCE–LIMX in the 10×10 SWT is completed. The following is an abridged procedure for starting up the SysID Rack from a power off state:

1. Press power rocker switch on the SysID Rack to on. The rocker switch indicator light will illuminate when power is on.
 - a. Let the target go through its boot-up process
 - b. Let the host go through its boot-up process
2. Start MathWorks MATLAB software on the host.
3. On the host and within MATLAB:
 - a. Open the target model that was developed using Simulink software.
 - (1) Compile it.
 - (2) Download it to the target.

- b. Start the target process.
- c. Open the host model that was developed using Simulink software and start it.
4. On the host, open and start the host GUI software code that streamlines the flow of instructions from the operator to the target.
5. Finally, on the dSPACE computer, press the power rocker switch to the on position. Then press the reset momentary switch on the dSPACE reset panel.

At this point, because of the default state of the SRPRs, the signal source for the HMC set-point ports is the facility controller. To transfer control to the SysID Rack, the state of the SRPRs must be changed. However, prior to making these state changes, care must be taken to ensure that a step change in actuator position will not occur when the SRPR changes state. To meet this concern, the SysID Rack actuator control set points are each set to a value that equals the current actuator position, as defined by converting the actuator feedback potentiometer signal to engineering units using calibration curves. With the SysID Rack set-point value set to apply signals to the HMCs that are consistent with the current actuator positions, the SRPR can be commanded to change state. After all SRPR states are set to allow SysID Rack signals to pass to the HMCs, the SysID Rack is ready to start conducting experiments on the CCE-LIMX in the 10x10 SWT.

The illustration in Figure 8 is an experiment signal flow map (host-target-dSPACE and then to the CCE-LIMX testbed effectors). Yellow arrows signify the path of actuator feedback signals and high-speed dynamic pressure sensors from the PFI signal conditioners, through the target, and to the host. The white arrows signify the paths of experiment instructions from the host, through the target, through the

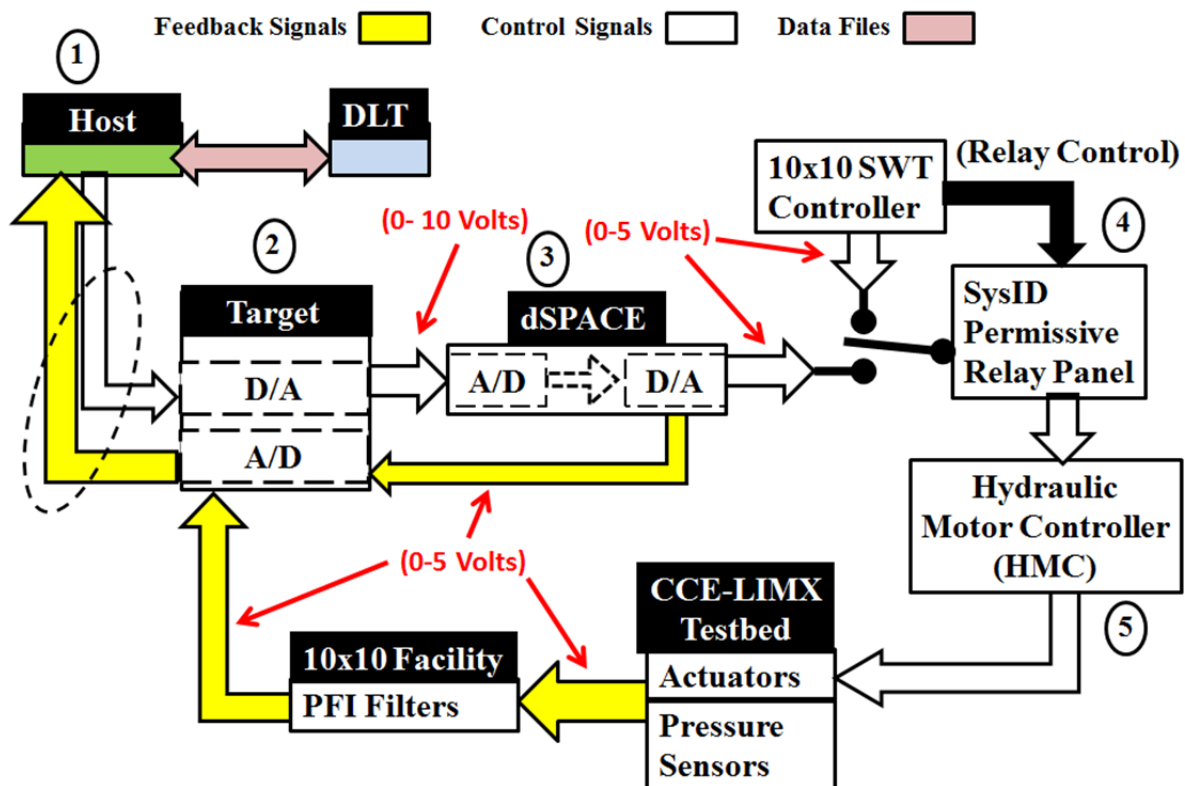


Figure 8.—SysID Rack signal flow for a typical Phase-2 SysID experiment. A CCE-LIMX actuator command signal is generated from the host (1) to the target D/A boards, (2) the command signal is passed through the dSPACE system, (3) when the 10x10 SWT facility relay panel, (4) selects the dSPACE system, the command signal is passed to the HMC controller(s), and (5) which in turn controls a hydraulic valve for moving the desired hardware to its designated position. Confirmation of actuator movement is fed back, through PFI filters, to the target and then host. At this point, the data can be saved and uploaded to the DTL.

dSPACE and on to the CCE–LIMX effector HMCs. When the SRPR panel, element 4 in Figure 8, is configured to pass SysID Rack signals, the dSPACE system signals are passed to the HMCs (element 5 in Fig. 8). The double-sided magenta arrow represents the communication link between the host and the DTL for file transfers between the computer systems. The black arrow is included to illustrate that the facility controller controls the states of the SRPRs on the actuator relay panel.

SysID Rack Experiment

One experiment type, stability transient index (S_{ti}) experiments (Ref. 7), required the use of the bypass doors. A bypass door, as illustrated in Figure 9, consists of a slotted plate and a slotted tray that lay atop of the plate. The piston rod moves, or slides, the slotted tray over the plate. When the slots in the tray are lined up with the slots in the plate, the door is fully open. The S_{ti} experiments require one door, or multiple combinations of the doors, to start with the door(s) partially open and move towards close-off and then back to the starting position again. The door position is defined as the door tray position with respect to the plate with units of inches: 0.0 in. has the doors closed and 0.75 in. has the doors fully open.

For these experiments, the commanded door position trace resembles a biased cosine wave and is mathematically described in Equation (1) with respect to time.

$$y(t) = y_0 + \frac{\Delta y}{2}(\cos(2\pi ft) - 1) \quad (1)$$

The desired door position, with respect to time, is y (in), the initial door position is y_0 (in), the magnitude of door position displacement is Δy (in), and f is the pulse frequency (Hz). The illustrations in Figure 10 are traces of signals recorded with the SysID Rack while performing an S_{ti} experiment. The experiment represented in Figure 10 only required the use of one door, door 4. Illustrated in Figure 10(a) is the desired pulse pattern for door 4. For this pattern, the initial door position was at 0.35 in., the pulse amplitude was 0.3 in., and the time scales in this illustration have been normalized. The top right illustration in Figure 10(b) is a trace representative of the signal that was passed from the SysID Rack target to the dSPACE system while performing this experiment. Since the computational hardware communicates by transmitting and receiving voltage signals, the engineering units (inches) describing the desired test pattern were converted to voltage values within a ± 10.0 -V range. Because of the electrical wiring for door 4, a voltage signal decrease moves the door slotted tray towards close-off and a voltage signal increase further opens the door area. Under normal operation, which was the case while recording the data illustrated in Figure 10, the dSPACE system scales the input voltage signals and outputs an equivalent 0.0 to +5.0-V signals to the SRPR panel where the signal is further directed to the HMC. This dSPACE generated signal was also recorded on the target A/D channels. The illustration in Figure 10(c) is a trace reconstructed from the data file that represents the voltage signal from the dSPACE system. Finally, the illustration in Figure 10(d) is a trace representing a copy of the voltage data recorded from the door 4 feedback potentiometer during this experiment. Again, the units are volts with a range from 0.0 to +5.0 and a calibration curve is needed to convert the voltage values to inches. Figure 10 clearly illustrate the SysID Rack was fully capable of carrying out the S_{ti} - type experiments. Additional testing showed that the SysID Rack was fully capable of carrying out all of the experiments.

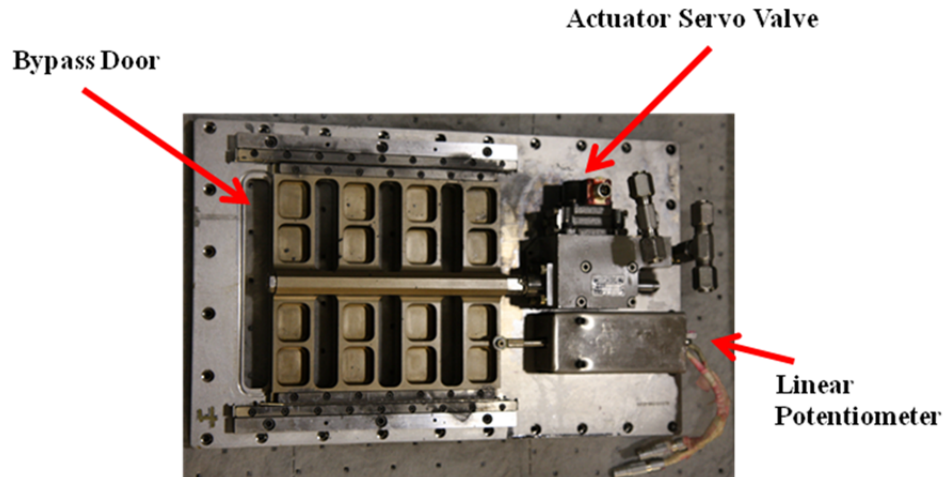


Figure 9.—One of four CCE-LIMX overboard bypass doors that are mounted at the aft end of the LSFP diffuser. These doors are designed to operate up to 100 Hz by controlling hydraulic fluid flow through an actuator servovalve. A linear potentiometer, for each bypass door, is used to provide bypass door positioning feedback signals to the SysID Rack.

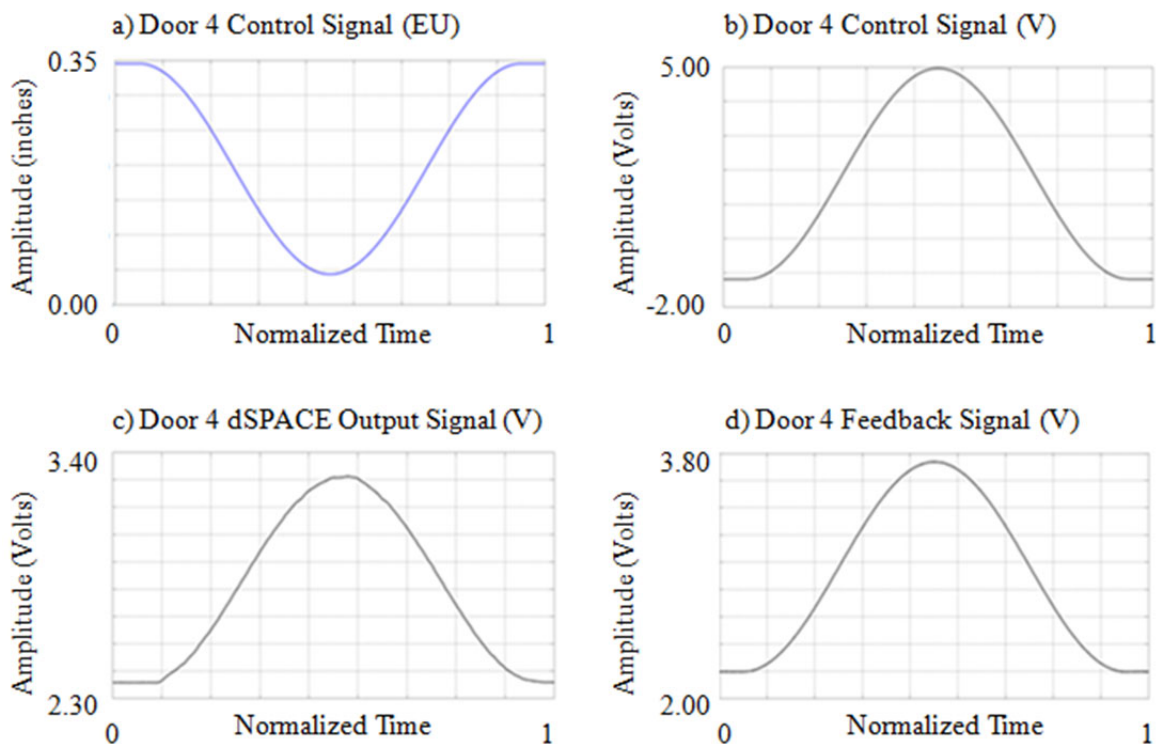


Figure 10.—Time normalized for a negative going pulse on door 4. Figure 10(a) shows the control signal for this experiment, measurement in inches. This control signal from the SysID Rack's target is shown in Figure 10(b), voltage span of ± 10.0 . Figure 10(c) is the output of the dSPACE system for this experiment with a range from 0.0 to +5.0 V. Finally, Figure 10(d) is the feedback signal (0.0 to +5.0 V) from the CCE-LIMX door 4 actuator feedback potentiometer.

SysID Rack Performance

Over an 8-month period from Aug. 29, 2011, to May 4, 2012, 651 dynamic experiments were conducted on the CCE–LIMX, at various operating conditions that included the following perturbation response tests: step, staircase, sinusoidal pulse, sinusoidal sweep, and constant sinusoid (Refs. 8 and 9). All experiments were conducted in the 10×10 SWT at Mach 3 (156 experiments) and simulated Mach 4 conditions (495 experiments). The experimental results database includes steady-state measurements of all flow-path pressure sensors and actuator positions before and after each experiment, and dynamic data acquired during the tests, using the SysID Rack, with a sample rate of 2.5 kHz. The SysID Rack hardware and software performed very well during the testing enabling a fast and safe pace for testing. Furthermore, the SysID Rack was useful for demonstrating inlet mode transition at both Mach 3 and simulated Mach 4 conditions. The data collected will be used to (1) Identify the frequency range where a closed-loop control system is needed to enhance the inlet stability margin and (2) Determine control design linear models. The control design models (CDMs) will be used to support controls design for closed-loop control of the CCE–LIMX simulating a hypersonic vehicle propulsion system mode transition.

Summary

This document presented the hardware and peripheral components used to build a data acquisition (DAQ) and control instrument rack (System Identification (SysID Rack)) to support Combined Cycle Engine Large-Scale Inlet for Mode Transition Experiments testbed experiments in the NASA Glenn 10- by 10-Foot Supersonic Wind Tunnel (10×10 SWT). All hardware and peripheral components were selected based on the following SysID Rack design requirements: safely and effectively move multiple actuators individually or synchronously; sample and save effector control and position sensor feedback signals; automate control of actuator positioning based on a mode transition schedule; sample and save pressure sensor signals; and perform DAQ and control processes operating at 2.5 KHz. Included were descriptions of component hardware and their specifications, functionality, and system interface. Also, the SysID Rack and 10×10 SWT effector signal flow list was provided along with a SysID Rack experiment setup and example and rack overall performance. Combining the selected hardware as described in this document resulted in the SysID Rack being more than capable of performing all tasks in real time with an update rate of 2.5 KHz. With the SysID Rack, all system identification experiments were completed in a timely and organized fashion. The experiments were coordinated with the SysID Rack and the experiment data was recorded on the SysID Rack. The SysID Rack was clearly a useful tool to meet the project objectives.

Appendix—System Identification Rack Signal Flow Tables

This appendix describes the signal paths between the System Identification (SysID) Rack and the Combined-Cycle Engine Large-Scale for Mode Transition Experiment (CCE–LIMX) testbed. All SysID Rack signals for the hydraulic machine controllers (HMCs) are products of the target process. The target process applies signals to digital-to-analog (D/A) board ports, which are wired to the dSPACE (dSPACE GmbH) analog-to-digital (A/D) ports via the SysID Rack target screw terminal boards and a dSPACE input Bayonet Neill-Concelman (BNC) connector panel. The dSPACE process reads the A/D ports, converts them to a 0.0- to +5.0-V range, and applies the converted values to D/A ports. The dSPACE D/A ports are wired from an output BNC connector panel to the following two locations: A BNC panel fabricated to accept signals from the dSPACE system for the SysID Rack permissive relay (SRPR) source gates and the target A/D screw terminal boards. While an experiment is under the SysID Rack control, the SRPR will pass the dSPACE signals to the HMCs. Along with the dSPACE control signals, CCE–LIMX testbed actuator feedback signals and the high-speed pressure transducer signals, conditioned with the Precision Filters, Inc. (PFI), instruments, are applied to the target A/D ports, by way of the target A/D screw terminal boards, where they are sampled and recorded.

The screw terminal boards, one for each data acquisition (DAQ) board, are labeled according to their peripheral component interface (PCI) board bus and slot number location. Because the two D/A boards are identical, they share the same PCI bus number; however, they have different slot number locations. Table A1 is a listing of connections to route signals from the target to the nine HMCs. The first column is a counter with 1 through 9 pertaining to the effectors, 10 being the sense line, and 11 being the signal from the dSPACE reset panel momentary push button. The “Location” column identifies the D/A channel as being a National Instruments Corporation (NI) board that occupies PCI bus number 7, slot 12 for the first board and slot 13 for the second. The “Contact” column identifies the actual screw terminal and pin number assignment for the signal D/A channel. The “Device label” column labels the target signal. In this column, the “SP” indicates the signal is a set point for a specific effector. The dSPACE system “A/D” column identifies the dSPACE A/D port assigned to read the target signals. Finally, the dSPACE system “D/A” column identifies the dSPACE output port that is connected to the SRPR source gates for each effector. The ports on the dSPACE input and output (I/O) panels are labeled as defined in the last two

TABLE A1.—CCE–LIMX TESTBED ACTUATOR CONTROL SIGNAL LIST

	Location	Contact	Device label	dSPACE system, A/D	dSPACE system, D/A
1	NI- Slot (7,12)	22/DAC0, 0	SP_Door1	Vin-1	Vout-1
	NI- Slot (7,12)	55			
2	NI- Slot (7,12)	21/DAC0, 1	SP_Door2	Vin-2	Vout-2
	NI- Slot (7,12)	54			
3	NI- Slot (7,12)	57/DAC0, 2	SP_Door3	Vin-3	Vout-3
	NI- Slot (7,12)	23			
4	NI- Slot (7,12)	25/DAC0, 3	SP_Door4	Vin-4	Vout-4
	NI- Slot (7,12)	58			
5	NI- Slot (7,12)	60/DAC0, 4	SP_LS_Ramp	Vin-5	Vout-5
	NI- Slot (7,12)	26			
6	NI- Slot (7,12)	28/DAC0, 5	SP_Splitter	Vin-6	Vout-6
	NI- Slot (7,12)	61			
7	NI- Slot (7,12)	30/DAC0, 6	SP_HS_MFP	Vin-7	Vout-7
	NI- Slot (7,12)	63			
8	NI- Slot (7,12)	65/DAC0, 7	SP_HS_Cowl	Vin-8	Vout-8
	NI- Slot (7,12)	31			
9	NI- Slot (7,13)	22/DAC1, 0	SP_LS_MFP	Vin-9	Vout-9
	NI- Slot (7,13)	55			
10	NI- Slot (7,13)	21/DAC1, 1	CPU_Overload	Vin-10	N/A
	NI- Slot (7,13)	54			
11	dSPACE Panel	N/A	dSPACE Reset	Vin-11	N/A

columns in Table A1. For example, the first entry in Table A1 is a signal from a NI board located in the target. The NI board occupies PCI bus number 7 and slot number 12. The signals on the NI board, contact numbers 22 and 55 corresponding with D/A bank 0, are HMC set-point signals from the target process for controlling bypass door 1. These signals are applied to the dSPACE A/D Vin-1 channel. The dSPACE system D/A output channel with HMC set-point signals for bypass door 1, Vout-1, is applied to a source gate on the SRPR panel associated with bypass door 1.

Table A2 is a listing of the dSPACE D/A output port connections to the target A/D ports. The “Location” column in Table A2 identifies the PCI slot nomenclature as occupied by United Electronics International (UEI) boards. The “Contact” and “Device label” columns are similar to as described for Table A1. For Table A2, the AIN is the analog input number on the UEI board that senses the dSPACE D/A ports. The “SP” designation under the “Device label” column represents the set point. The “Device label” column also indicates the effector associated with the set-point signal. The “Description” column identifies the signal source and voltage range, all from dSPACE and ranging from 0.0 to +5.0 V. For example, the first entry in Table A2 indicates the UEI board occupies PCI bus number 8 and slot number 15. The set-point signal is applied to the UEI board contact AIN29. The fifth column in this table indicates the signal range will be between 0.0 and +5.0 V.

The positions of the nine effectors are also recorded by the target. Feedback signal routing from the actuator position sensor potentiometers are documented in Table A3. The column labels in Tables A2 and A3 are identical. The “FB” designation in the labels under the “Device label” column represents “Feedback.” For the signals documented in Table A3, all signals are from the PFI instruments with a range from 0.0 to +5.0 V.

In Table A2, nine dSPACE output (0.0 to +5.0 V) actuator feedback signal wires are labeled and terminated to the SysID Rack United Electronics International (UEI) screw terminal board. The screw terminal board is interfaced with a UEI A/D peripheral component interface (PCI) board. This PCI board is located on the target’s PCI bus (bus number 8) at slot location 15.

Table A3 identifies nine CCE–LIMX actuator feedback signals after being routed through the Glenn 10- by 10-Foot Supersonic Wind Tunnel facility PFI filters. The PFI filtered outputs are labeled and wired to the SysID Rack’s UEI screw terminal board contacts. This screw terminal board is interfaced with its corresponding target UEI (A/D) PCI board, PCI bus (bus number 8) at slot location 15.

TABLE A2.—THE DSPACE ACTUATOR CONTROL FEEDBACK SIGNAL LIST

	Location	Contact	Device label	Description
1	UEI-Slot (8,15)	AIN29	SP_Door1	0.0 to + 5.0V from dSPACE
2	UEI-Slot (8,15)	AIN30	SP_Door2	0.0 to + 5.0V from dSPACE
3	UEI-Slot (8,15)	AIN31	SP_Door3	0.0 to + 5.0V from dSPACE
4	UEI-Slot (8,15)	AIN32	SP_Door4	0.0 to + 5.0V from dSPACE
5	UEI-Slot (8,15)	AIN33	SP_Ramp	0.0 to + 5.0V from dSPACE
6	UEI-Slot (8,15)	AIN34	SP_Splitter	0.0 to + 5.0V from dSPACE
7	UEI-Slot (8,15)	AIN35	SP_HS_MFP	0.0 to + 5.0V from dSPACE
8	UEI-Slot (8,15)	AIN36	SP_HS_Cowl	0.0 to + 5.0V from dSPACE
9	UEI-Slot (8,15)	AIN37	SP_LS_MFP	0.0 to + 5.0V from dSPACE

TABLE A3.—CCE–LIMX TESTBED ACTUATOR FEEDBACK SIGNAL LIST

	Location	Contact	Device label	Description
1	UEI-Slot (8,15)	AIN0	FB_Ramp	0.0 to + 5.0V from PFI
2	UEI-Slot (8,15)	AIN1	FB_Splitter	0.0 to + 5.0V from PFI
3	UEI-Slot (8,15)	AIN2	FB_HS_Cowl	0.0 to + 5.0V from PFI
4	UEI-Slot (8,15)	AIN3	FB_Door1	0.0 to + 5.0V from PFI
5	UEI-Slot (8,15)	AIN4	FB_Door2	0.0 to + 5.0V from PFI
6	UEI-Slot (8,15)	AIN5	FB_Door3	0.0 to + 5.0V from PFI
7	UEI-Slot (8,15)	AIN6	FB_Door4	0.0 to + 5.0V from PFI
8	UEI-Slot (8,15)	AIN7	FB_LS_MFP	0.0 to + 5.0V from PFI
9	UEI-Slot (8,15)	AIN8	FB_HS_MFP	0.0 to + 5.0V from PFI

Table A4 is a listing of the Kulite (Kulite Semiconductor Products, Inc.) pressure sensor feedback signals that are used to record the dynamic data from the high- and low-speed flow paths. The “Locations” and “Contact” labels are the same as what was used in Tables A2 and A3. Documented in the column under the “Device label” heading is the Kulite identification tag. The following are acronyms included in this column to distinguish each Kulite transducer by its physical location: “S” for signal applied to the SysID Rack, “LRB” for low-speed ramp bleed, “HRB” for high-speed ramp bleed, “HCI” for high-speed cowl (wall assembly) interior, “HII” for high-speed (isolator assembly) interior, and “LCB” for low-speed cowl bleed. The number at the end of each acronym identifies the Kulite sensor position in inches, away from the reference point: the leading edge of the precompression ramp. The Kulite sensors and the actuator feedback sensor signals are routed through the PFI signal conditioners. As indicated in the fifth column under the “Description” label, the PFI output range is 0.0 to +5.0 V.

In Table A1 the SysID Rack outputs nine actuator control signals (1 to 9) and two step-changing trigger signals (10 to 11). The target incorporates two NI D/A PCI boards. Each board is identified by its location within the target PCI bus structure (bus number 7), slot number 12 or 13. These NI boards are wired to NI screw terminal board contacts. The screw terminal board contact wires are labeled and interfaced with the dSPACE system’s input A/D board. Each incoming signal into the dSPACE system is scaled from ± 10.0 V to 0.0 to +5.0 V and routed to its corresponding dSPACE output.

In Table A4 the CCE–LIMX Kulite pressure transducer signals are wired to the Glenn 10- by 10-Foot Supersonic Wind Tunnel facility PFI filters. From the PFI filters, these signals are labeled and wired to the SysID Rack’s UEI A/D screw terminal board contacts. The screw terminal board is interfaced with its corresponding target UEI PCI slot (A/D) board, PCI bus (bus number 8) at slot location 15.

TABLE A4.—CCE–LIMX PRESSURE SENSOR SIGNAL LIST

	Location	Contact	Device Label	Description
1	UEI-Slot (8,15)	AIN9	SLRB1540	0.0 to + 5.0V from PFI
2	UEI-Slot (8,15)	AIN10	SHRB1445	0.0 to + 5.0V from PFI
3	UEI-Slot (8,15)	AIN11	SLRB1586	0.0 to + 5.0V from PFI
4	UEI-Slot (8,15)	AIN12	SHCI1445	0.0 to + 5.0V from PFI
5	UEI-Slot (8,15)	AIN13	SLRB1660	0.0 to + 5.0V from PFI
6	UEI-Slot (8,15)	AIN14	SHCI1520	0.0 to + 5.0V from PFI
7	UEI-Slot (8,15)	AIN15	SLRB1800	0.0 to + 5.0V from PFI
8	UEI-Slot (8,15)	AIN16	SHCI1580	0.0 to + 5.0V from PFI
9	UEI-Slot (8,15)	AIN17	SLCB1500	0.0 to + 5.0V from PFI
10	UEI-Slot (8,15)	AIN18	SHCI1680	0.0 to + 5.0V from PFI
11	UEI-Slot (8,15)	AIN19	SLCB1660	0.0 to + 5.0V from PFI
12	UEI-Slot (8,15)	AIN20	SHCI1800	0.0 to + 5.0V from PFI
13	UEI-Slot (8,15)	AIN21	SHRB1150	0.0 to + 5.0V from PFI
14	UEI-Slot (8,15)	AIN22	SHII1930	0.0 to + 5.0V from PFI
15	UEI-Slot (8,15)	AIN23	SHRB1300	0.0 to + 5.0V from PFI
16	UEI-Slot (8,15)	AIN24	SHII2130	0.0 to + 5.0V from PFI
17	UEI-Slot (8,15)	AIN25	SHII2255	0.0 to + 5.0V from PFI
18	UEI-Slot (8,15)	AIN26	SLRB1880	0.0 to + 5.0V from PFI
19	UEI-Slot (8,15)	AIN27	SLCB2160	0.0 to + 5.0V from PFI
20	UEI-Slot (8,15)	AIN28	SLRB2160	0.0 to + 5.0V from PFI

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REPORT DOCUMENTATION PAGE				Form Approved OMB No. 0704-0188	
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1. REPORT DATE (DD-MM-YYYY) 01-08-2013		2. REPORT TYPE Technical Memorandum		3. DATES COVERED (From - To)	
4. TITLE AND SUBTITLE Combined Cycle Engine Large-Scale Inlet for Mode Transition Experiments: System Identification Rack Hardware Design				5a. CONTRACT NUMBER	
				5b. GRANT NUMBER	
				5c. PROGRAM ELEMENT NUMBER	
6. AUTHOR(S) Thomas, Randy; Stueber, Thomas, J.				5d. PROJECT NUMBER	
				5e. TASK NUMBER	
				5f. WORK UNIT NUMBER WBS 599489.02.07.03.07.11.02	
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration John H. Glenn Research Center at Lewis Field Cleveland, Ohio 44135-3191				8. PERFORMING ORGANIZATION REPORT NUMBER E-18657	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration Washington, DC 20546-0001				10. SPONSORING/MONITOR'S ACRONYM(S) NASA	
				11. SPONSORING/MONITORING REPORT NUMBER NASA/TM-2013-217864	
12. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified-Unlimited Subject Category: 07 Available electronically at http://www.sti.nasa.gov This publication is available from the NASA Center for AeroSpace Information, 443-757-5802					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT The System Identification (SysID) Rack is a real-time hardware-in-the-loop data acquisition (DAQ) and control instrument rack that was designed and built to support inlet testing in the NASA Glenn Research Center 10- by 10-Foot Supersonic Wind Tunnel. This instrument rack is used to support experiments on the Combined-Cycle Engine Large-Scale Inlet for Mode Transition Experiment (CCE-LIMX). The CCE-LIMX is a testbed for an integrated dual flow-path inlet configuration with the two flow paths in an over-and-under arrangement such that the high-speed flow path is located below the low-speed flow path. The CCE-LIMX includes multiple actuators that are designed to redirect airflow from one flow path to the other; this action is referred to as "inlet mode transition." Multiple phases of experiments have been planned to support research that investigates inlet mode transition: inlet characterization (Phase-1) and system identification (Phase-2). The SysID Rack hardware design met the following requirements to support Phase-1 and Phase-2 experiments: safely and effectively move multiple actuators individually or synchronously; sample and save effector control and position sensor feedback signals; automate control of actuator positioning based on a mode transition schedule; sample and save pressure sensor signals; and perform DAQ and control processes operating at 2.5 KHz. This document describes the hardware components used to build the SysID Rack including their function, specifications, and system interface. Furthermore, provided in this document are a SysID Rack effectors signal list (signal flow); system identification experiment setup; illustrations indicating a typical SysID Rack experiment; and a SysID Rack performance overview for Phase-1 and Phase-2 experiments. The SysID Rack described in this document was a useful tool to meet the project objectives.					
15. SUBJECT TERMS Hypersonic; Combined cycle engine large-scale inlet for mode transition experiments					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UU	18. NUMBER OF PAGES 32	19a. NAME OF RESPONSIBLE PERSON STI Help Desk (email: help@sti.nasa.gov)
a. REPORT U	b. ABSTRACT U	c. THIS PAGE U			19b. TELEPHONE NUMBER (include area code) 443-757-5802

